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Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

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Washington, D. C. 20231

Case Docket No. 0325.00273
Date: September 24, 1999

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): Paul Scott and S. Babar Raza

For: METHOD, ARCHITECTURE AND CIRCUITRY FOR CONTROLLING PULSE WIDTH IN A PHASE AND/OR FREQUENCY DETECTOR

Enclosed are:

1. X Specification (11 pages); Claims (5 pages); Abstract (1 page)

2. X 5 sheets of informal drawings.

3. X Oath or Declaration Total Pages 2
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP) of prior application no.: _____

6. X An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$760.00
Total Claims	16	0	x $ 18.00	$ 0.00
Indep. Claims	3	0	x $ 78.00	$ 0.00
Mult. Dep. Claims			$260.00	$ 0.00

SUB-TOTAL $760.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ..... $ ____

X Assignment Recordal Fee ($40.00) ..... $ 40.00

TOTAL $800.00

X A check in the amount of $800.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

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021363

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CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL417952854US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on September 24, 1999.

By: Mary Donna Berkley

Mary Donna Berkley

Respectfully submitted,

By _____

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METHOD, ARCHITECTURE AND CIRCUITRY FOR CONTROLLING PULSE WIDTH IN A PHASE AND/OR FREQUENCY DETECTOR

Field of the Invention

The present invention relates to a single frequency serial link system generally and, more particularly, to a method and/or architecture for eliminating a receive PLL in a single frequency serial link system.

Background of the Invention

FIG. 1 shows a block diagram of a circuit 10 illustrating a conventional PLL system. The circuit 10 generally comprises a receive circuit 12 and a transmit circuit 14. The transmit circuit 14 generally comprises a number of outputs 16a-16n that may present information (i.e., serial data) about a number of ports Port1-PortN. The receive circuit 12 may have a number of inputs 18a-18n that may receive the information from the transmitter circuit 14. The receive circuit 12 generally comprises a deserializer circuit 20, a receive PLL 22 and a selectable multiplexer 24. The selectable multiplexer 24 presents a signal to the receive PLL in response to the information received at the inputs 18a-18n. The receive PLL presents a first signal to an input 26 of the

deserializer 20 and a second signal to an input 28 of the deserializer 20. The deserializer 20 may present a parallel data word at an output 30 in response to the signals received at the inputs 26 and 28.

The transmitter circuit 14 generally comprises a divide circuit 40, a transmit PLL 42, a serializer circuit 44 and a selectable demultiplexer 46. The serializer 44 generally receives a parallel data word at an input 50 and a signal BIT_CLOCK at an input 52. The serializer 44 generally presents a signal to an input 54 in response to the parallel data received at the input 50 and the bit clock received at the input 52. The transmit PLL 42 generally presents the signal BIT_CLOCK in response to a reference clock signal REFCLK received at an input 56 and a signal BYTE_CLOCK received at an input 58. The divide circuit 40 generally converts the signal BIT_CLOCK to the signal BYTE_CLOCK. Data is received by the transmitter circuit 14 on a parallel bus and is serialized using the signal BIT_CLOCK. Once the data is serialized, the data is sent through the selectable demultiplexer 46 to one of the ports Port1-PortN.

For the receive side, the data received by one of the ports Port1-PortN of the receive circuit 12. The data is passed

through the selectable multiplexer 24 to the receive PLL 22. The receive PLL 22 recovers a clock signal from the incoming serial data, and presents the serial data and the recovered clock to the inputs 26 and 28 of the deserializer circuit 20. The deserializer circuit 20 presents the parallel data at the output 30. The circuit 10 has two PLLs (i.e., the receive PLL 22 and the transmit PLL 42) one for the receive circuit 12 and one for the transmit circuit 14.

Summary of the Invention

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals. The second circuit may be configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

The objects, features and advantages of the present invention include providing a serial communication link that may (i) eliminate lock time and/or (ii) be implemented using a single PLL.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a diagram of a conventional circuit for single frequency serial link system;

FIG. 2 is a block diagram of a preferred embodiment of the present invention;

FIG. 3 is a circuit diagram of a phase generation and select clock circuit of FIG. 2;

FIG. 4 is a detailed block diagram of a phase comparator circuit of FIG. 2; and

FIG. 5 is a block diagram of an alternate embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 2, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 generally comprises a receive block (or circuit) 102 and a transmit block (or circuit) 104. The receive block 102 generally comprises a deserializer circuit 106, a

selectable multiplexer 108, a phase generation and selection block (or circuit) 110 and a phase comparator block (or circuit) 112. The selectable multiplexer circuit 108 may have a number of inputs 114a-114n that may receive information (e.g., serial data) from a number of ports (e.g., Port1-PortN). The selectable multiplexer circuit 108 may present a signal (e.g., SIN_CUR) at an output 116 and a signal (e.g., SIN_NEXT) at an output 118. The signals SIN_CUR and SIN_NEXT may be serial data from the current port PORTa-PORTn and the next port PORTa-PORTn.

The phase comparator circuit 112 may have an input 120 that may receive the signal SIN_NEXT and a number of inputs 122a-122n that may receive a number of signals (e.g., phase signals PHASEa-PHASEn) from the phase generator and select circuit 110. The phase comparator 112 may have an output 124 that may present a signal (e.g., PHASE_SELECT) in response to the signals PHASEa-PHASEn and the signal SIN_NEXT. The phase generation and select circuit 110 may have an input 126 that may receive a signal (e.g., BIT_CLOCK) from the transmitter circuit 104 and an input 128 that may receive the signal PHASE_SELECT. The phase generation and select circuit 110 may present a signal (e.g., CLK_CUR) to an input 130 of the deserializer circuit 106 in response to the signal

PHASE_SELECT and the signal BIT_CLOCK. The deserializer circuit 106 may have an input 132 that may receive the signal SIN_CUR. The deserializer circuit 106 may present parallel data at an output 134 in response to the signal CLK_CUR and the signal SIN_CUR.

The transmit circuit 104 generally comprises a divide circuit 150, a transmit PLL circuit 152, a deserializer circuit 154 and a selectable demultiplexer circuit 156. The transmit PLL circuit 152 may receive a reference clock signal (e.g., REF_CLK) at an input 160 and a clock signal (e.g., BYTE_CLOCK) at an input 162. The transmit PLL circuit 152 may present a clock signal (e.g., BIT_CLOCK) at an output 164 in response to the reference clock signal REF_CLK and the signal BYTE_CLOCK. The divide circuit 150 may present the signal BYTE_CLOCK at an output 166 in response to the signal BIT_CLOCK received at an input 168. The signal BIT_CLOCK may also be presented, through an output 170, to an input 172 of the receive circuit 102. The deserializer circuit 154 may present a signal to an input 174 of the selectable demultiplexer circuit 156 in response to the signal BIT_CLOCK received at an input 176 and the parallel data received at an input 178. The selectable demultiplexer circuit 156 may present serial data at a number of outputs 180a-180n.

The selectable multiplexer circuit 108 may be configured to send data on two ports, one to data destination port (e.g., the output 116) and the other to the look-ahead port (e.g., the output 118). The look-ahead output 118 may communicate data in the next slot time. Since the circuit 100 is generally implemented in a single frequency serial link system, the same reference clock REF_CLK may be used by all the ports Port1-PortN.

In the receiver circuit 102, the receive PLL (of FIG. 1) is eliminated and is generally replaced by the phase generator and select circuit 110 and the phase comparator circuit 112. The selectable multiplexer 108 may select two of the N ports Port1-PortN and (i) pass the current serial data as the signal SIN_CUR and (ii) pass serial data for the next slot time as the signal SIN_NEXT. The signal SIN_CUR may be the data that is currently being received by the selectable multiplexer 108. The signal SIN_NEXT may be the look-ahead data used by the phase comparator circuit 112 to pick the phase for a slot time after an end of packet is encountered.

The phase comparator circuit 112 may generate the signal PHASE_SELECT in response to a comparison of the signal SIN_NEXT to the different phase signals PHASEa-PHASEn received from the phase

generator and select circuit 110. The phase generator and select circuit 110 may generate a number of phases of the signal BIT_CLOCK as the clock phase signals PHASEa-PHASEn. The clock phase signals PHASEa-PHASEn may be presented to the inputs 122a-122n of the phase comparator circuit 112. The phase comparator circuit 112 may determine the particular clock phase signal PHASEa-PHASEn that may correspond to the particular serial data received at the inputs 114a-114n.

Referring to FIG. 3, a circuit diagram of the phase generation and select circuit 110 is shown. The phase generation and select circuit 110 may comprise a clock multiplexer 200 and a number of buffers 202a-202n. The buffers 202a-202n may each be connected in series with the signal BIT_CLOCK. A respective output of each of the buffer circuits 202a-202n may be presented to one of a number of inputs 204a-204n of the multiplexer 200. For example, the input 204a may receive the signal BIT_CLOCK prior to any of the buffer circuits 202a-202n. The input 204b may receive the output of the buffer circuit 202a. The input 204n may receive the output of the buffer circuit 202n. The outputs of the buffers 202a-202n may be the phase signals PHASEa-PHASEn, respectively. Additionally, the phase signals PHASEa-PHASEn presented to the

inputs 204a-204n may also be presented to the outputs 123a-123n. For example, the signal presented to the input 204a may also be presented to the output 123a. The multiplexer 200 may be configured to present the signal CLK_CUR in response to the phase signals PHASEa-PHASEn and the signal PHASE_SELECT.

The signal BIT_CLOCK may pass through different delay elements 202a-202n to generate different phases of the signal BIT_CLOCK. The phase comparator circuit 112 may select the phase that may correspond to the current serial data in response to the signal PHASE_SELECT received at the input 128.

Referring to FIG. 4, a detailed block diagram of the phase comparator circuit 112 is shown. The phase comparator circuit 112 generally comprises a number of shift register blocks (or circuits) 300a-300n, a comparison logic circuit 302 and a phase select storage circuit 304. Each of the shift register blocks 300a-300n may receive the signal SIN_NEXT from the input 120 and one of the signals PHASEa-PHASEn from the inputs 122a-122n. Each of the shift register blocks 300a-300n may present a multi-bit signal to an input 310a-310n of the comparison logic block 302. The comparison logic block 302 may present a signal to an input 312 of the phase select storage block 304. The phase select storage

block 304 may present the signal PHASE_SELECT in response to the signal received at the signal 312 and one or more of the clock phase signals PHASEa-PHASEn received at an input 314.

The signal SIN_NEXT is generally presented to each of the shift register blocks 300a-300n, which are generally clocked with different clock phase signals PHASEa-PHASEn. The data from each of the shift register blocks 300a-300n may be compared with a known expected value. The shift register blocks 300a-300n with the best match to one or more known values generally determines the phase of the incoming serial link Port1-PortN. The selected value is loaded into the phase select storage device 304 in the next slot time after the end of packet is encountered.

Referring to FIG. 5, a circuit 100′ illustrating an alternate embodiment of the present invention is shown. The circuit 100′ further comprises a phase storage device 400 and a multiplexer 402. The circuit 100′ may store the output of the phase comparator 112′ in the phase storage device 400 during an initialization of each port Port1-PortN. The value of the selected phase can then be passed to the phase generator and select circuit 110′ from the phase storage device 400, through the multiplexer 402, rather than continually calculating and generating the signal

PHASE_SELECT. When not calculating the signal PHASE_SELECT, the phase comparator circuit 112′ may be powered down. If any of the ports change phase, the particular port or the circuit 100′ may be reinitialized.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. An apparatus comprising:

a first circuit configured to present a parallel output data in response to (i) a first clock signal and (ii) one or more serial data signals; and

a second circuit configured to present said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

2. The apparatus according to claim 1, wherein said first clock signal comprises a bit clock signal.

3. The apparatus according to claim 1, wherein said second clock signal comprises a reference clock signal.

4. The apparatus according to claim 1, wherein said first circuit further comprises:

a third circuit configured to generate (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.

5. The apparatus according to claim 4, wherein said first circuit further comprises:

a phase comparator circuit configured to generate said phase select signal in response to said one or more select signals and one of said one or more serial data signals.

6. The apparatus according to claim 4, wherein said third circuit comprises a phase generation and select circuit.

7. The apparatus according to claim 4, wherein said first circuit includes a deserializer circuit configured to generate said parallel output data signal in response to said selected clock signal and another one of said one or more serial data signals.

8. The apparatus according to claim 7, wherein said first circuit further comprises:

a multiplexer configured to generate (i) said one of said one or more serial data signals and (ii) said another one of said one or more serial data signals, in response to said one or more serial data signals.

9. A circuit comprising:

means for generating a parallel output data in response to (i) a first clock signal and (ii) one or more serial data signals; and

means for generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

10. A method for controlling a pulse width in a phase and/or frequency detector comprising the steps of:

(A) generating a parallel output data in response to (i) a first clock signal and (ii) one or more serial data signals; and

(B) generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal, wherein said first clock signal is configured to control said pulse width.

11. The method according to claim 10, wherein said first clock signal comprises a bit clock signal.

12. The method according to claim 10, wherein said second clock signal comprises a reference clock signal.

13. The method according to claim 10, wherein step (A) further comprises the sub-step of:

generating (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.

14. The method according to claim 13, wherein step (A) further comprises the sub-step of:

generating said phase select signal in response to said one or more select signals and one of said one or more serial data signals.

15. The method according to claim 14, wherein step (A) further comprises the sub-step of:

generating said parallel output data signal in response to said selected clock signal and another one of said one or more serial data signals.

16. The method according to claim 15, further comprising the step of:

generating said one of said one or more serial data signals and said another one of said one or more serial data signals, in response to said one or more serial data signals.

ABSTRACT OF THE DISCLOSURE

An apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals. The second circuit may be configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

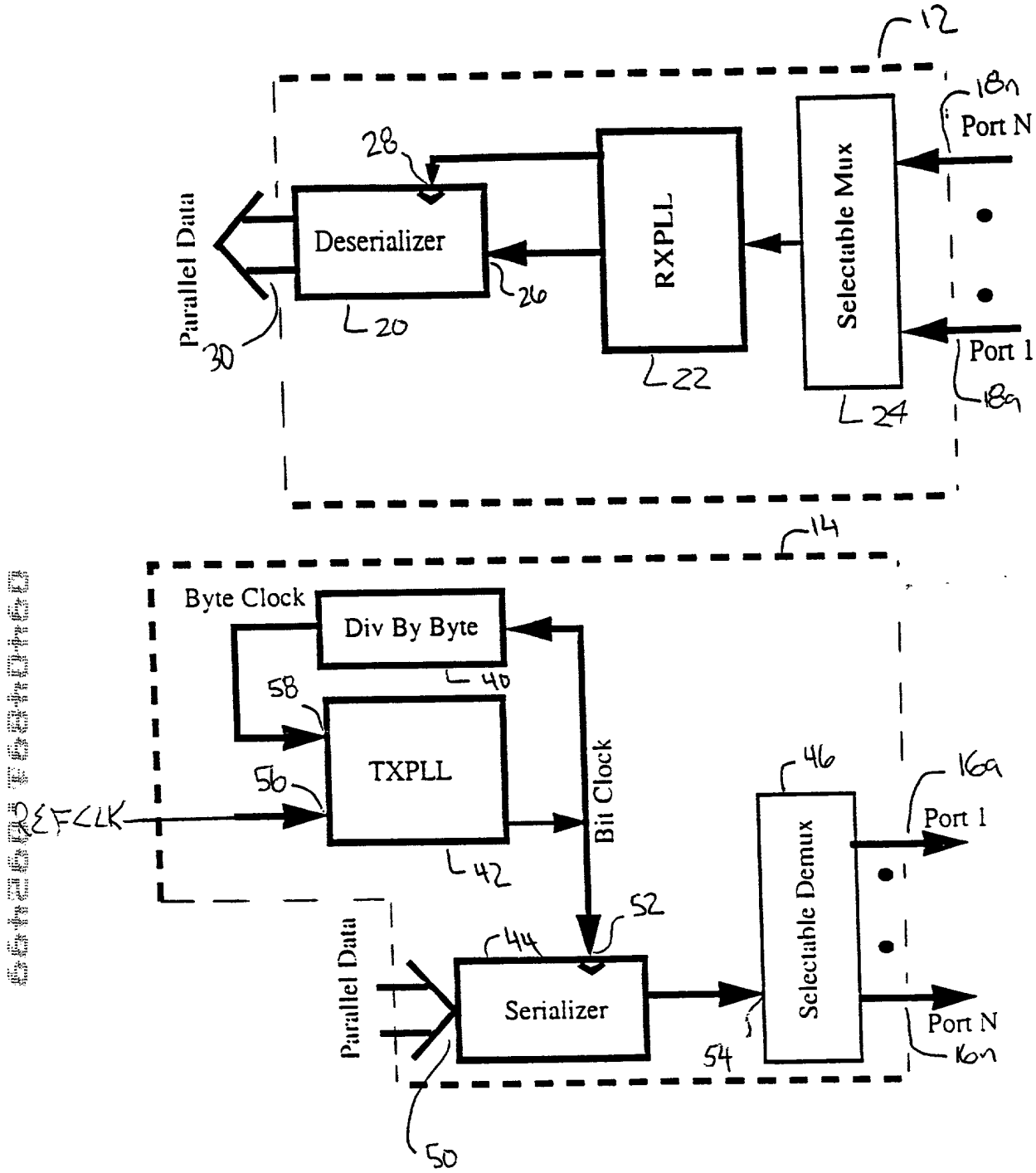
10
12
18n
Port N
28
Deserializer
RXPLL
Selectable Mux
Parallel Data
26
20
22
24
30
Port 1
18a
14
Byte Clock
Div By Byte
40
58
TXPLL
56
REFCLK
42
Bit Clock
46
16a
Port 1
52
44
Serializer
Selectable Demux
Parallel Data
54
Port N
16n
50

FIG.1

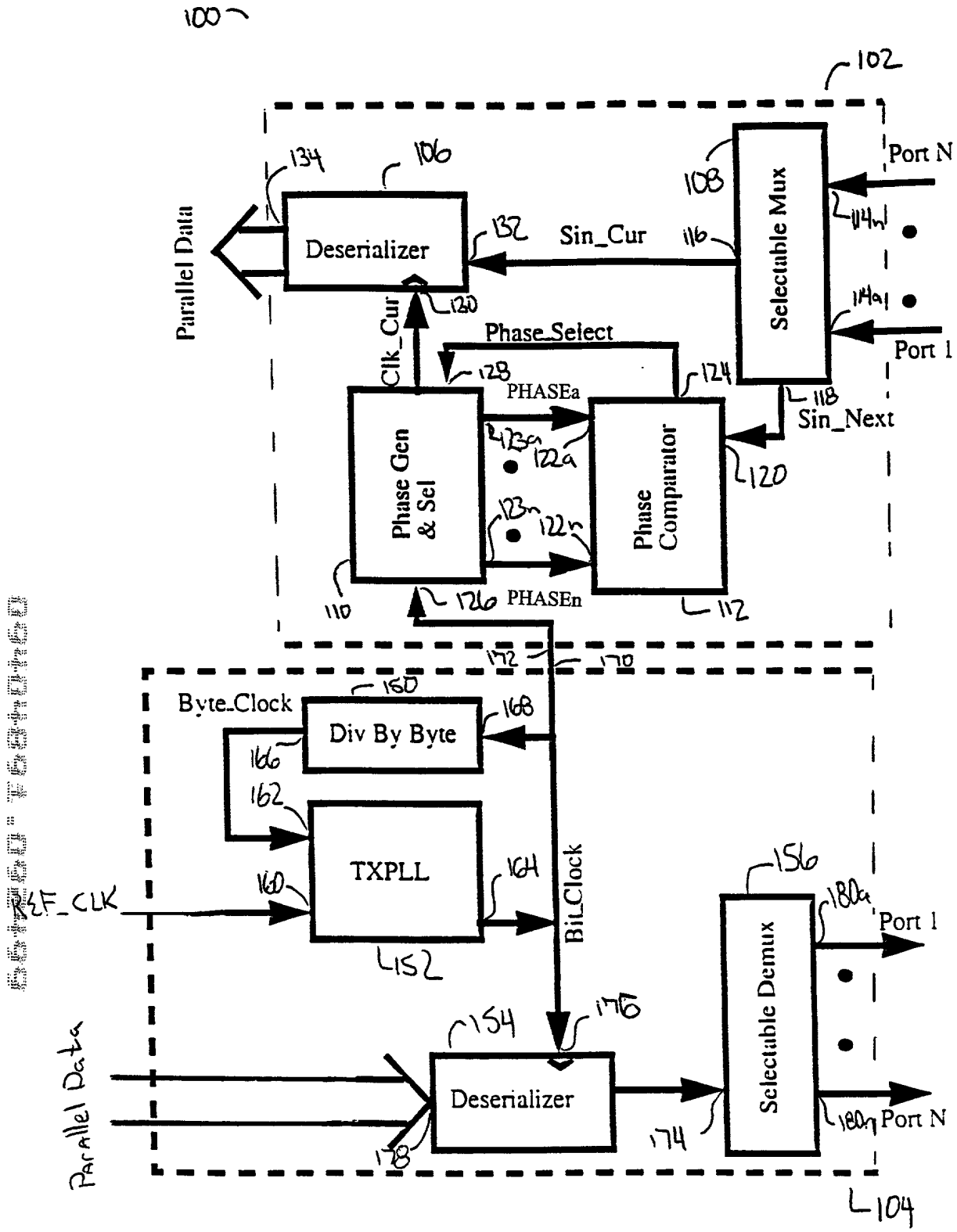
100
102
Parallel Data
Deserializer
106
134
132
Sin_Cur
116
Selectable Mux
108
Port N
114n
114a
Port 1
120
Clk_Cur
Phase_Select
128
124
PHASEa
118
Sin_Next
Phase Gen & Sel
Phase Comparator
123a
122a
123n
122n
120
110
126
PHASEn
112
172
170
Byte_Clock
160
Div By Byte
168
166
162
TXPLL
164
160
REF_CLK
152
BitClock
156
180a
Port 1
Selectable Demux
154
176
Parallel Data
Deserializer
178
174
180n
Port N
104

FIG.2

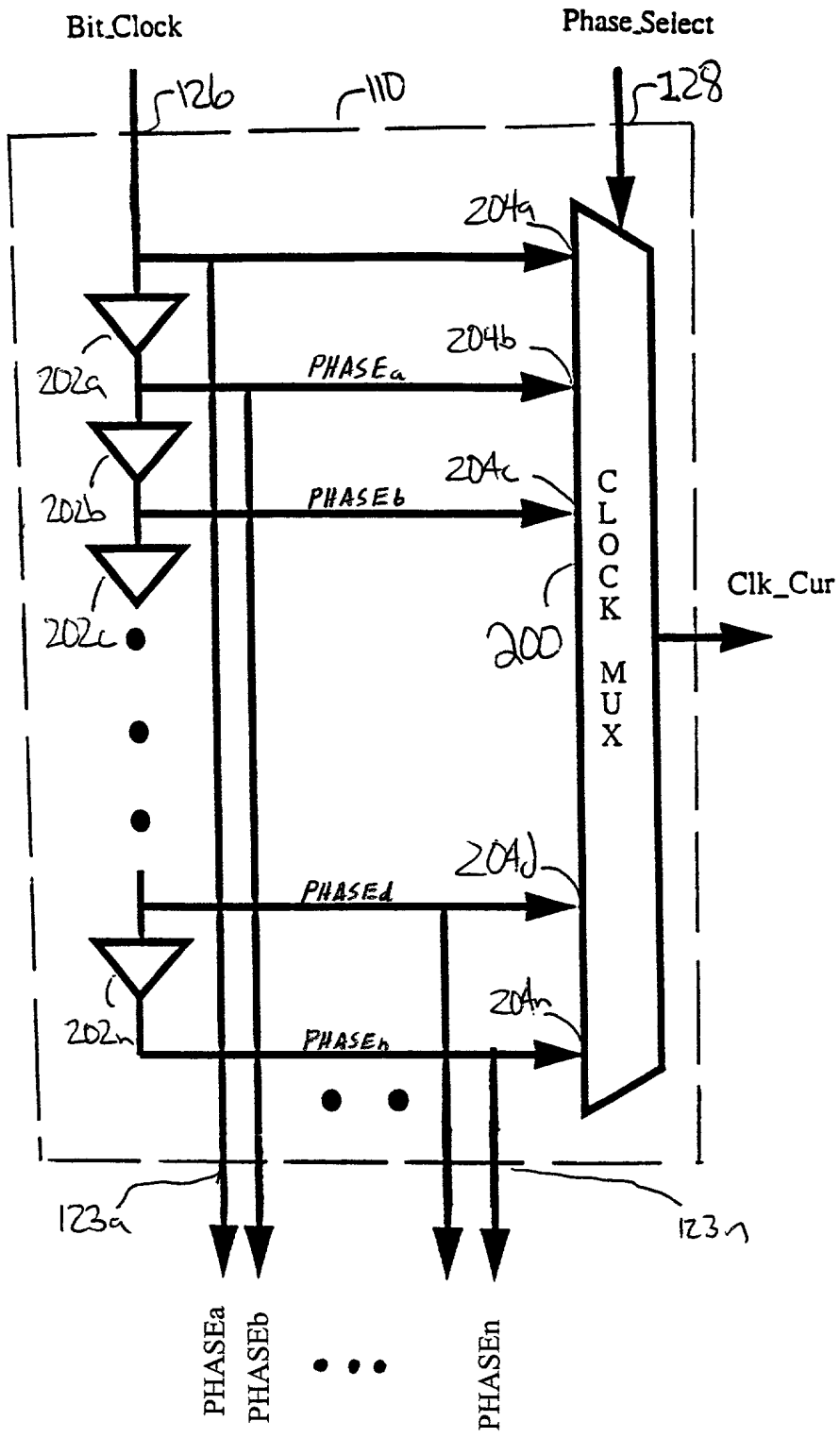
Bit_Clock
Phase_Select
126
110
128
204a
202a
204b
PHASEa
202b
204c
PHASEb
CLOCK MUX
Clk_Cur
202c
200
204d
PHASEd
202n
204n
PHASEn
123a
123n
PHASEa
PHASEb
PHASEn

FIG.3

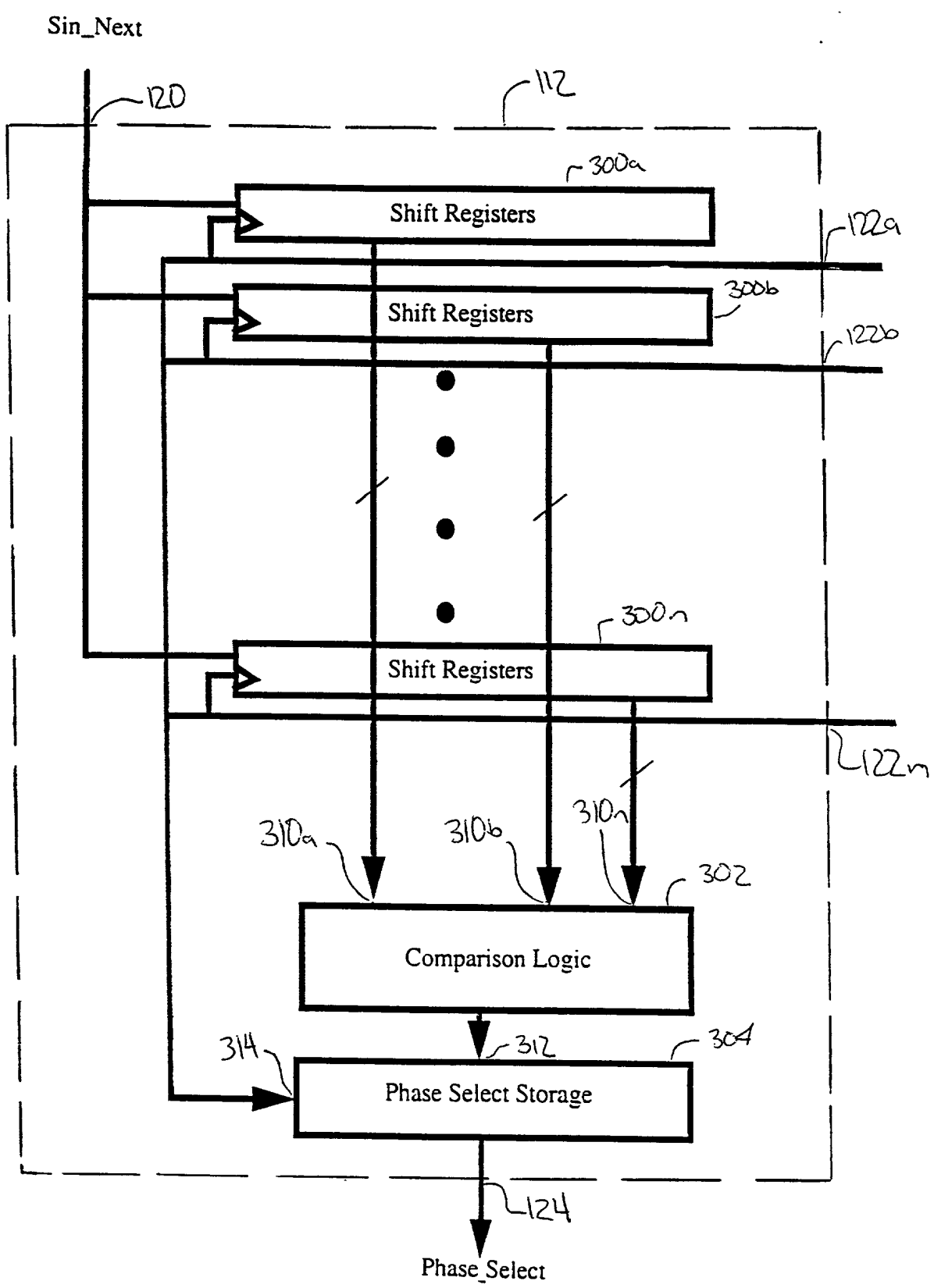
Sin_Next
120
112
300a
Shift Registers
122a
300b
Shift Registers
122b
300n
Shift Registers
122n
310a
310b
310n
302
Comparison Logic
312
304
314
Phase Select Storage
124
Phase_Select

FIG.4

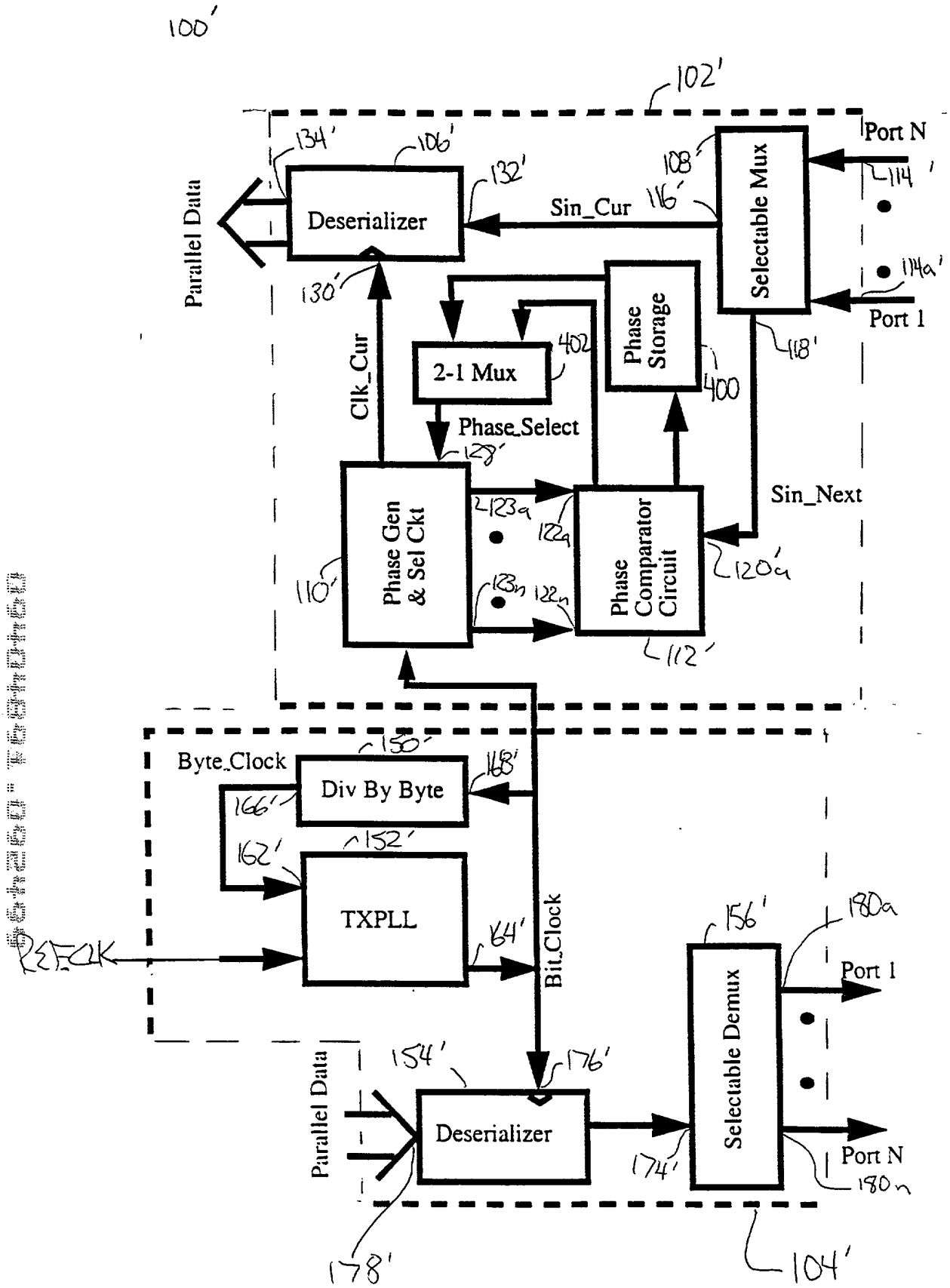
100'
102'
Parallel Data
134'
106'
Deserializer
132'
Sin_Cur
116'
108'
Selectable Mux
Port N
114'
114a'
Port 1
130'
Clk_Cur
2-1 Mux
402
Phase Storage
400
418'
Phase_Select
128'
Phase Gen & Sel Ckt
110'
123a
122a
123n
122n
Phase Comparator Circuit
120'a
112'
Sin_Next
150'
Byte_Clock
Div By Byte
168'
166'
162'
152'
TXPLL
164'
REFCLK
Bit_Clock
156'
180a
Port 1
Selectable Demux
Port N
180n
154'
176'
Parallel Data
Deserializer
174'
178'
104'

FIG.5

Docket No. 0325.00273

DECLARATION, POWER OF ATTORNEY AND PETITION

We, the undersigned inventors, hereby declare that:

My residence, post office address and citizenship are given next to my name;

We believe that we are the first, original and joint inventors of the subject matter claimed in the application for patent entitled **"METHOD, ARCHITECTURE AND CIRCUITRY FOR CONTROLLING PULSE WIDTH IN A PHASE AND/OR FREQUENCY DETECTOR"**, which:

__X__ is submitted herewith;

_____ was filed on _____ as Application Serial No. _____ and amended on _____;

We have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

We acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. We also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

> compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or
>
> refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

We hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

We hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

We hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, we acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

We hereby appoint as our attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

021363

PATENT TRADEMARK OFFICE

We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

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